



KERSEMI

PRODUCT SUMMARY	
V _{DS} (V)	800
R _{DS(on)} (Ω)	V _{GS} = 10 V 3.0
Q _g (Max.) (nC)	78
Q _{gs} (nC)	9.6
Q _{gd} (nC)	45
Configuration	Single

FEATURES

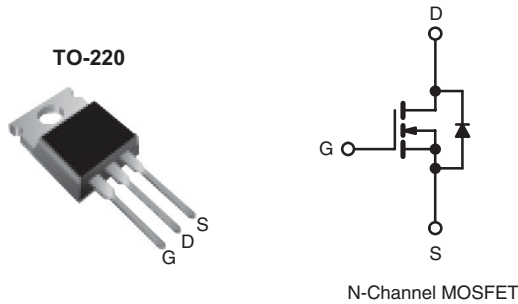
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available



DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRFBE30PbF
	SiHFBE30-E3
SnPb	IRFBE30
	SiHFBE30

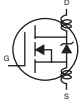

ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	800	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	I _D	T _C = 25 °C	A
			T _C = 100 °C	
Pulsed Drain Current ^a		I _{DM}	16	
Linear Derating Factor			1.0	W/°C
Single Pulse Avalanche Energy ^b		E _{AS}	260	mJ
Repetitive Avalanche Current ^a		I _{AR}	4.1	A
Repetitive Avalanche Energy ^a		E _{AR}	13	mJ
Maximum Power Dissipation	T _C = 25 °C	P _D	125	W
Peak Diode Recovery dV/dt ^c		dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d	
Mounting Torque	6-32 or M3 screw		10	
			1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 50 V, starting T_J = 25 °C, L = 29 mH, R_G = 25 Ω, I_{AS} = 4.1 A (see fig. 12).
- I_{SD} ≤ 4.1 A, dI/dt ≤ 100 A/μs, V_{DD} ≤ 600, T_J ≤ 150 °C.
- 1.6 mm from case.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		800	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	0.9	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$		-	-	100	μA
		$V_{DS} = 640\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 2.5\text{ A}^b$	-	-	3.0	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 100\text{ V}, I_D = 2.5\text{ A}^b$		2.5	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5		-	1300	-	pF
Output Capacitance	C_{oss}			-	310	-	
Reverse Transfer Capacitance	C_{rss}			-	190	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 4.1\text{ A}, V_{DS} = 400\text{ V},$ see fig. 6 and 13 ^b	-	-	78	nC
Gate-Source Charge	Q_{gs}			-	-	9.6	
Gate-Drain Charge	Q_{gd}			-	-	45	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 4.1\text{ A}$ $R_G = 12\text{ }\Omega, R_D = 95\text{ }\Omega,$ see fig. 10 ^b		-	12	-	ns
Rise Time	t_r			-	33	-	
Turn-Off Delay Time	$t_{d(off)}$			-	82	-	
Fall Time	t_f			-	30	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	4.1	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	16	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 4.1\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 4.1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	480	720	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.8	2.7	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



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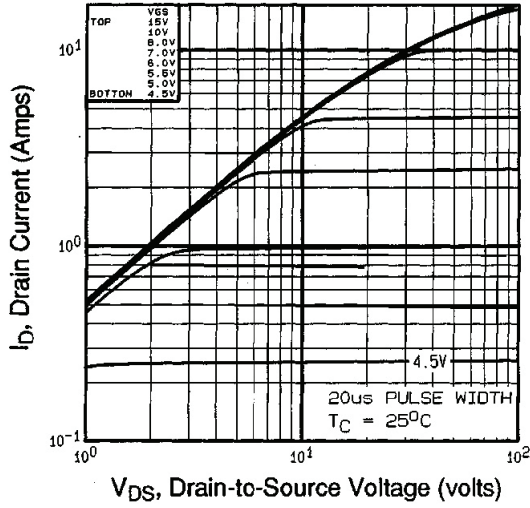


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ C$

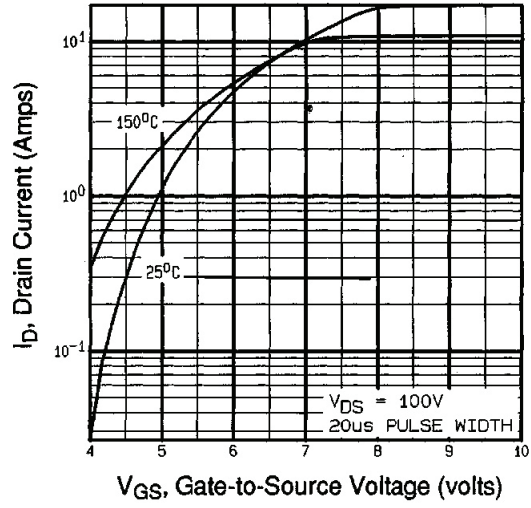


Fig. 3 - Typical Transfer Characteristics

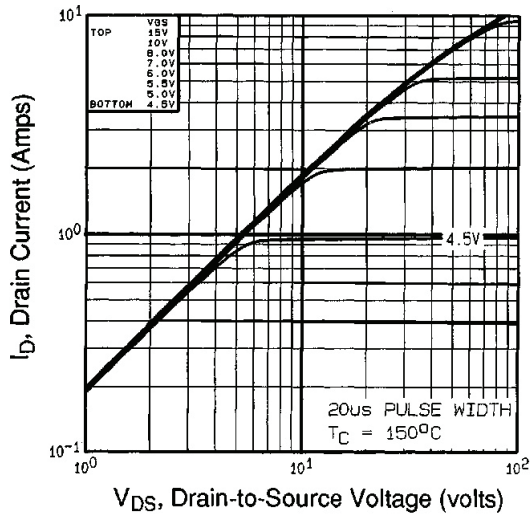


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ C$

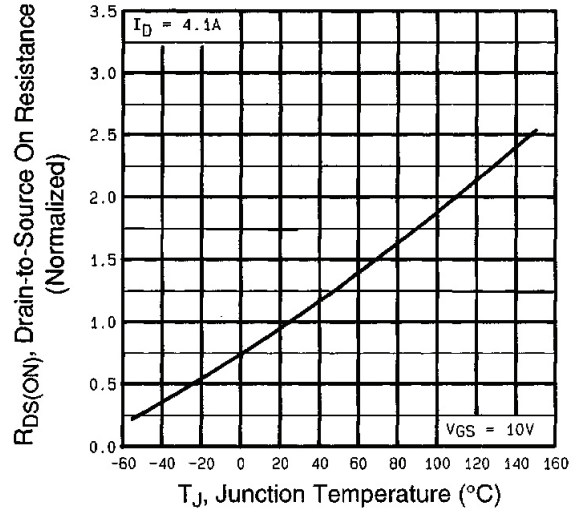


Fig. 4 - Normalized On-Resistance vs. Temperature

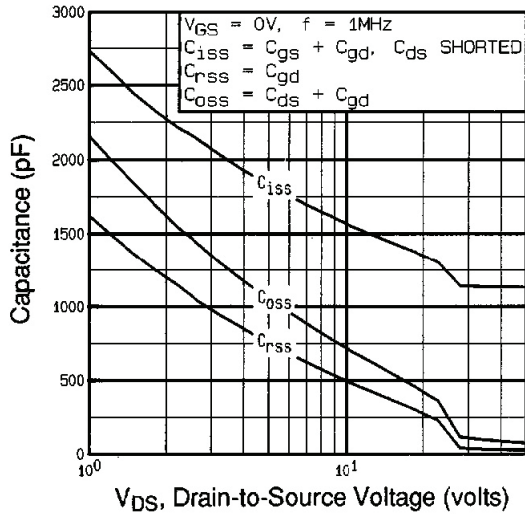


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

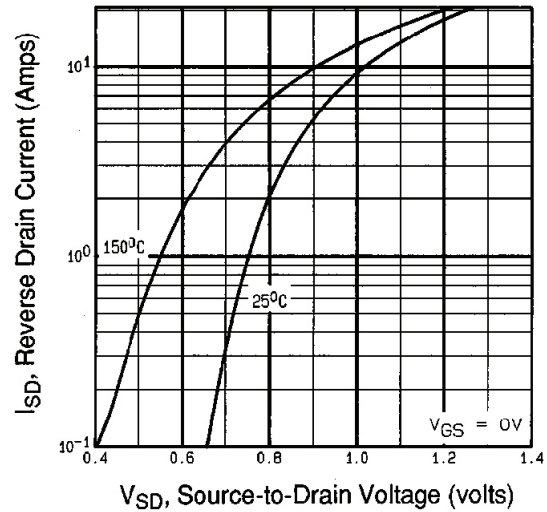


Fig. 7 - Typical Source-Drain Diode Forward Voltage

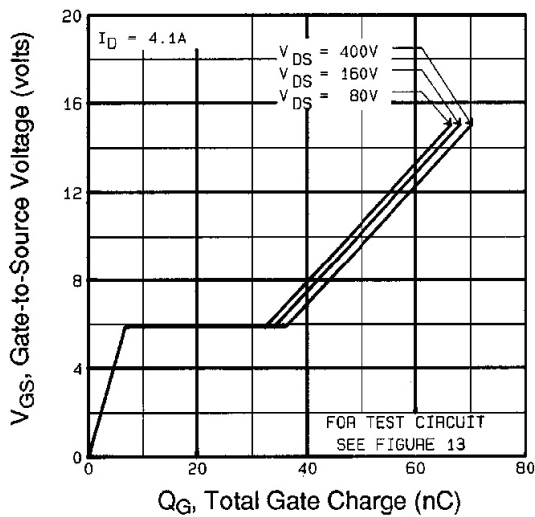


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

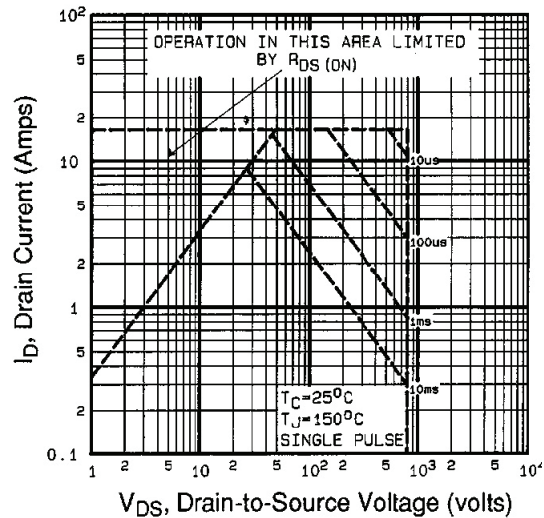


Fig. 8 - Maximum Safe Operating Area



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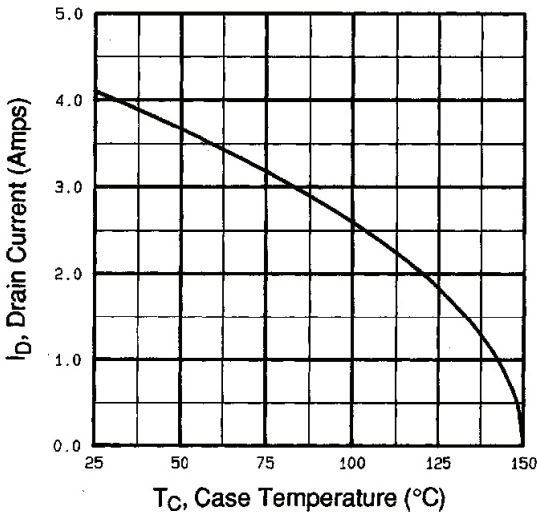


Fig. 9 - Maximum Drain Current vs. Case Temperature

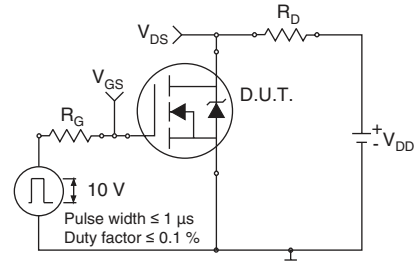


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

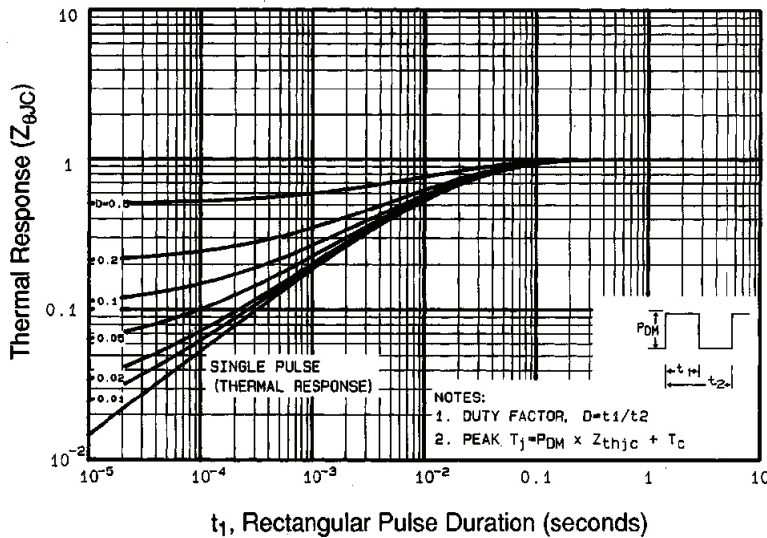


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

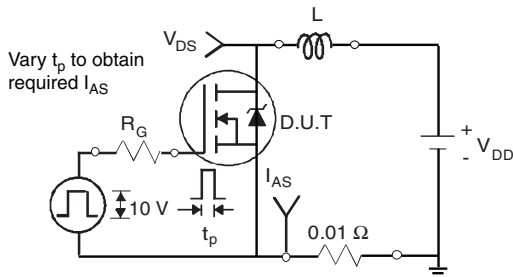


Fig. 12a - Unclamped Inductive Test Circuit

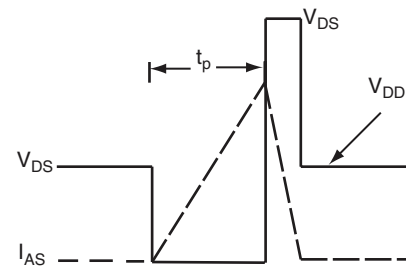


Fig. 12b - Unclamped Inductive Waveforms

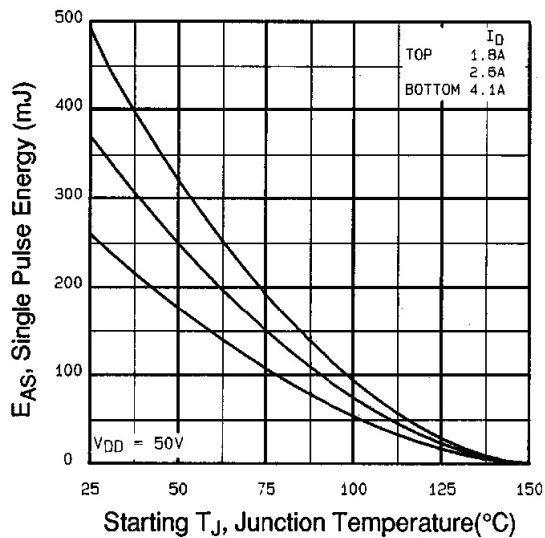


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

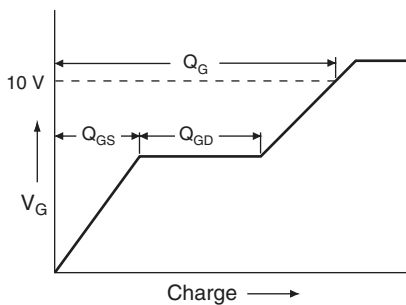


Fig. 13a - Basic Gate Charge Waveform

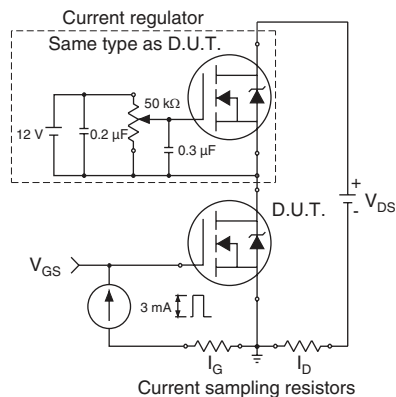
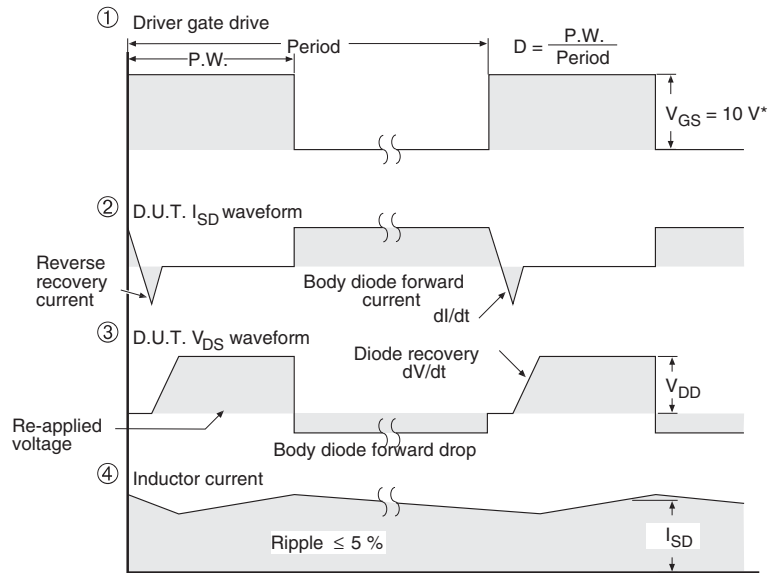
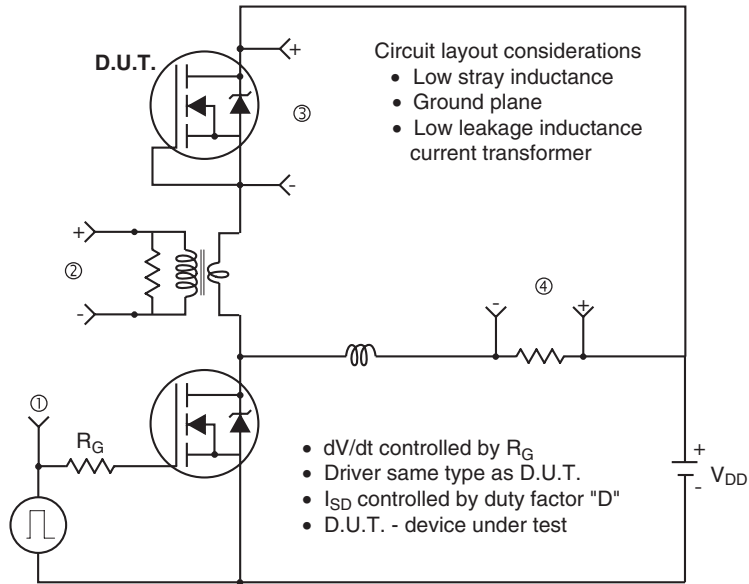


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel